

**A New Space Vector Modulation(SVM)
with Optimal Switching Sequence**

The need for control algorithm of low switching losses and harmonic distortion is becoming more and more urgent, especially when the high frequency devices are used in the power electronic systems. So a new space vector modulation (SVM) was introduced, which has the virtue of low switching losses and harmonic distortion. And the algorithm model was built to study its operation in Simulink. Simulation results, including the output voltage waveforms and the spectrum of the output line-to-line voltage, were given under various modulation indices and N (the ratio of carrier frequency to modulation wave frequency). The experiments of the algorithm had been carried out based on TMS320F2812 DSP. It is shown that the proposed SVM makes doubled calculations at specified switching frequency. And the output THD of it is better than that of 7-segment SVM.

Keywords: Space vector modulation; Switching sequence; Harmonic; Switching losses; Simulink.

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1. Introduction

The SVM control technique is widely used in the power electronic system, such as inverter and rectifier [1, 2]. Relative to the sinusoidal pulse width modulation (SPWM), SVM is more suitable for digital implementation and can increase the obtainable maximum output line voltage which approaches 70.7% of the DC link voltage in the linear modulation range. Moreover, it can obtain a better voltage total harmonic distortion factor.

When SVM is used to modulate the power electronic system, symmetric 7-segment switching sequence is a popular solution [3-5]. The switching frequency of the 7-segment SVM is the same as the sampling frequency of power electronic system. With the development of the power electronics, the high frequency power devices are extensively applied. But the higher the frequency, the higher the switching losses. A low switching losses control algorithm will help to increase the efficiency of power electronic application.

In this paper, an optimal SVM strategy with low switching losses was proposed. The model of it based on 3-phase 2-level inverter was constructed in Simulink, whose operation was studied. The experimental results validated the proposed algorithm.

¹ Corresponding author: Zhang Weifeng, zhangwf@szit.edu.cn, Department of Electronic and Communication Technology, Shenzhen Institute of Information Technology, Shenzhen 518172, China

2. Principles of SVM

We assume that there are only two independent variables in a 3-phase voltage system. Then the orthogonal coordinates can be used to represent the 3-phase voltage in the vector diagram. The three-phase-voltage vector can be expressed in matrix form as follows:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{AO} \\ v_{BO} \\ v_{CO} \end{bmatrix} \quad (1)$$

In SVM control algorithm, the 3-phase output voltage is represented by a reference voltage vector, which rotates at the angular velocity of $\omega = 2\pi f$. The SVM can use the combinations of switching states to approximate the locus of V_{ref} (the reference voltage vector). In practical application, the eight possible switching states of the inverter (Figure1) are represented as 2 zero vectors and 6 active vectors. The switching states and corresponding vectors are shown in Table1. The vector plane which is structured by the 6 active vectors (V_1 - V_6) is illustrated in Figure2. The rotating reference voltage vector can be synthesised in each switching cycle by switching the two adjacent active vectors and the zero vectors. The hexagon vector diagram framed by the 6 active vectors is equally divided into 6 sectors. In order to make f_{sw} (the effective switching frequency) a minimal value, the sequence of the switching between these vectors will be organized in such way that only one inverter leg is affected in every toggling step.

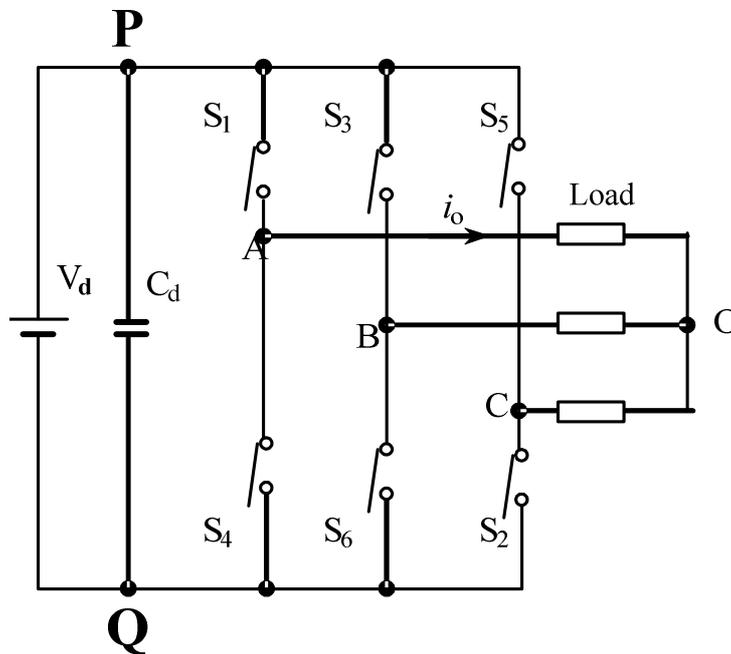


Figure 1 Three-phase inverter

Table 1 Switching states of the 2-level inverter

Space vector		Switching state	'On' switches S_i
Zero vector	V_7	[111]	1, 3, 5
	V_0	[000]	4, 6, 2
Active vector	V_1	[001]	4, 6, 5
	V_2	[010]	4, 3, 2
	V_3	[011]	4, 3, 5
	V_4	[100]	1, 6, 2
	V_5	[101]	1, 6, 5
	V_6	[110]	1, 3, 2

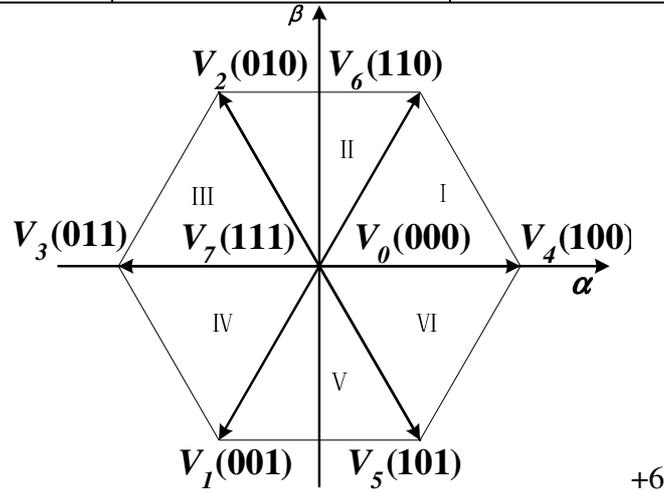


Figure 2 Vector plane frame

3. Proposed SVM

The sector judgment and dwelling time of active vector are the same as conventional scheme [5]. So we will only describe the switching sequence of the new scheme in details in this section.

The proposed scheme was designed as follows. Assuming the reference vector located in sector I, the first sampling point used the sequence V_4 - V_6 - V_7 , which goes counter-clockwise along the vertices of the sector, and then the next sampling point used V_6 - V_4 - V_0 , which goes clockwise. The counter-clockwise and clockwise sequences were used alternatively. The dwelling times of each sequence were calculated at the sampling frequency.

Figure 3 shows the proposed algorithm sequences of sector I in 2 sampling periods. It is clear in Figure 3 that there are only 0.5 switching actions in each sampling periods, which means the sampling frequency can be doubled at a certain switching frequency.

Two types of sequences, S_p and S_q , can be defined (Figure 3), where, S_p is the P -type sequence which contains P -type null vector $PPP(111)$, and S_q is q -type sequence containing null vector $QQQ(000)$. T_x and T_y should be swapped when the vector was located in even number sectors. Switch sequences were given in Table 2 for each sector.

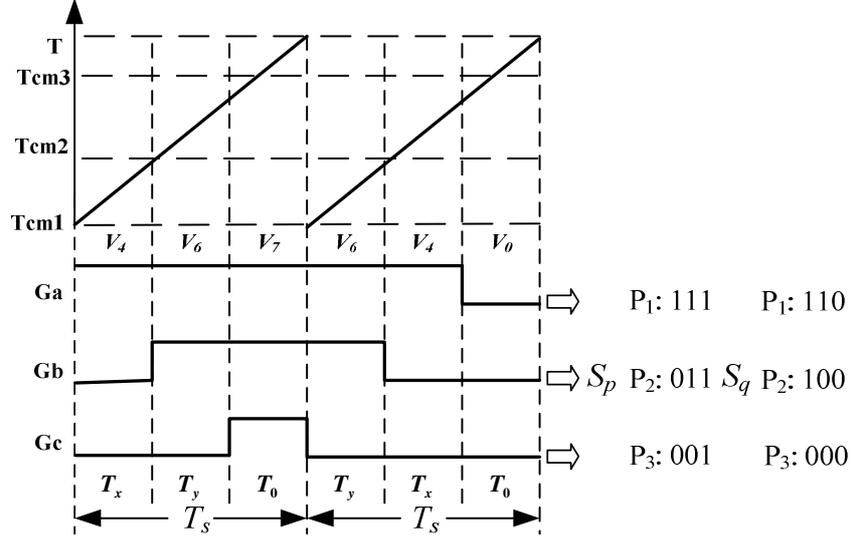


Figure 3 Alternative 3-segment switching sequence of sector I

Table 2 Switch sequences for all the 6 sectors

Sector	I	II	III	IV	V	VI
Sequences	$P_1P_2P_3$	$P_2P_1P_3$	$P_3P_1P_2$	$P_3P_2P_1$	$P_2P_3P_1$	$P_1P_3P_2$

4. Simulation results

Simulink model of the proposed SVM was built based on the above definition of switching sequences. The model had been run according to the following parameters sets: DC link voltage $V_d = 310V$, output line voltage frequency $f = 50Hz$, $R = 16.25\Omega$, $L = 0.25mH$.

4.1 DC bus voltage utilization

The operation in the linearity region or overmodulation region is determined by the modulation factor m , which is defined as:

$$m = \frac{\sqrt{3}V_{ref}}{V_d}$$

where, V_{ref} is the reference vector and V_d is the DC link voltage.

4.1.1 Linearity modulation

When $m = 1$ in the linearity region, the output line voltage value is the same as V_d which shown in Figure 4(a). If $m < 1$, the output line voltage is smaller than the maximum value

V_d as shown in Figure 4(b). So the proposed SVM can increase the utilization of DC bus voltage as 7-segment SVM^[5].

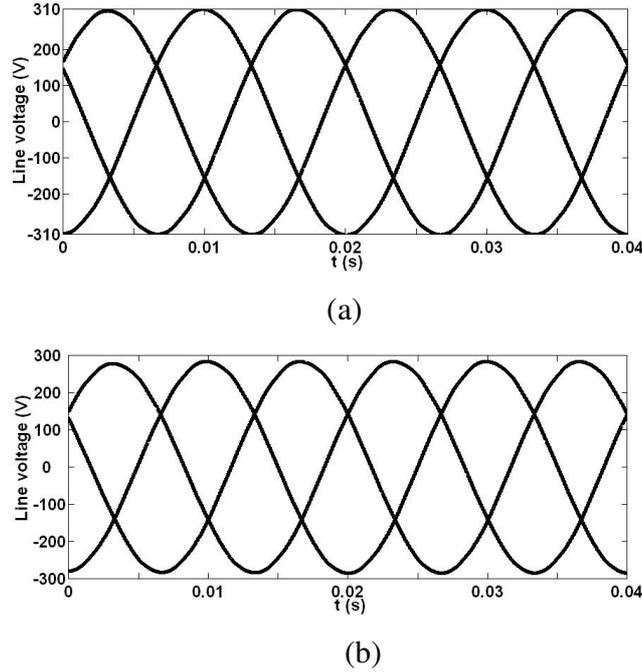


Figure 4 Output line voltage when $m \leq 1$

4.1.2 Overmodulation

The overmodulation region can be divided into two sections. If $\frac{V_d}{\sqrt{3}} \leq V_{ref} \leq \frac{2V_d}{3}$, the simulation results are shown in Figure 5(a). And when $V_{ref} > \frac{2V_d}{3}$, the simulation results are shown in Figure 5(b). It is shown that the maximum output line voltage could exceed the value of V_d . However, the maximum output line voltage changes little in the two sections.

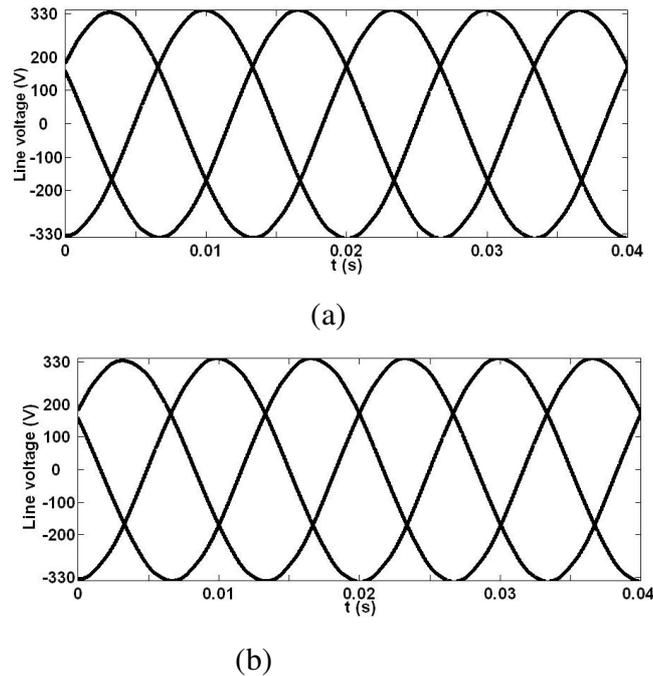
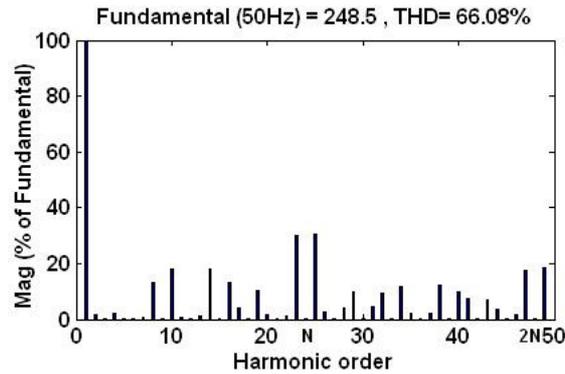


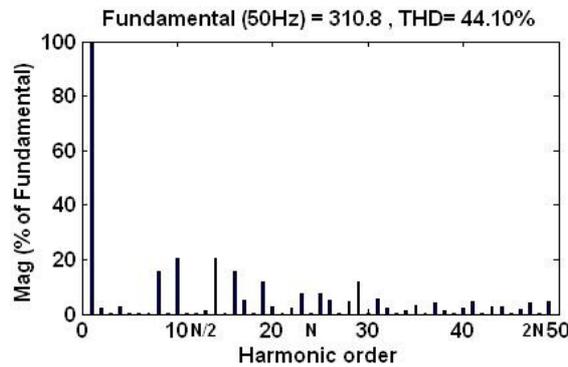
Figure 5 Output line voltage in overmodulation region

4.2 Analysis of output line voltage harmonic

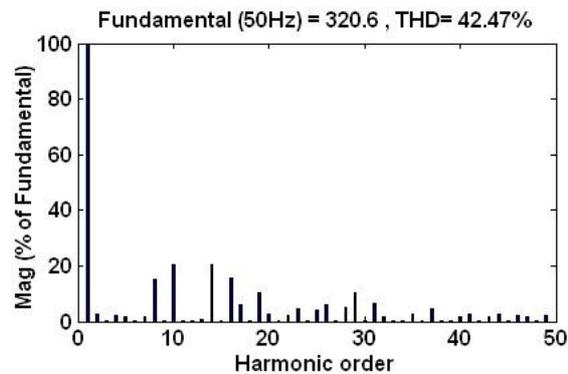
Figure 6 shows the spectrum of the output line voltage at different modulation indices (a: $m = 0.8$, b: $m = 1$, c: $m = 1.06$, d: $m = 1.16$). When the modulation index increases, the THD of the output voltage decreases. In the two overmodulation regions, the THD changes little. And the harmonics are centered at the multiples of N (the ratio of carrier frequency to modulation wave frequency), which is also a general phenomenon of SPWM schemes. But with the increase of m , the main harmonic region shifts to the low frequency. From Figure 6(a) ($N = 24$) and Figure 6(e) ($N = 12$), it is known that THD decreases when N increases.



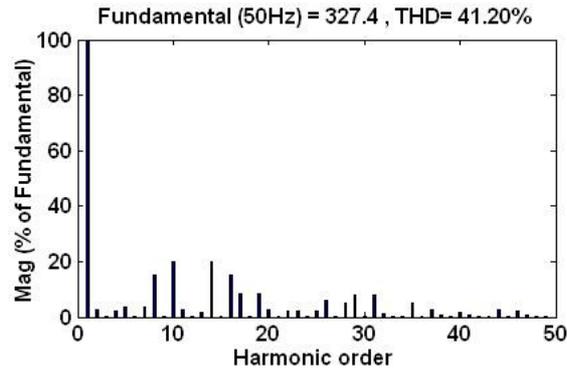
(a)



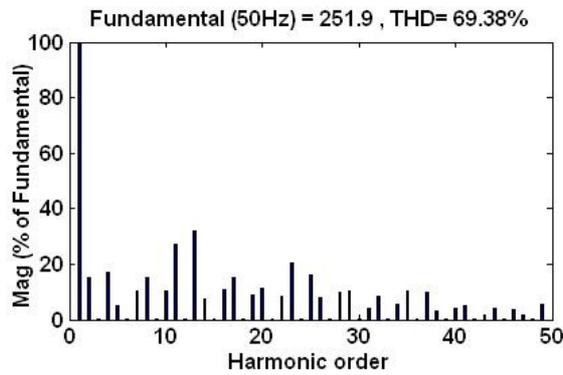
(b)



(c)



(d)



(e)

Figure 6 Harmonics spectrum of 3-segment SVM

4.3 Harmonic comparison between proposed SVM and popular SVM

Figure 7 shows the spectrum of the output line voltage of 7-segment SVM ($N=12, m=0.8$). Compared to Figure 6(a), It is clear that THD of 7-segment SVM is higher than that of proposed SVM under the same switching frequency.

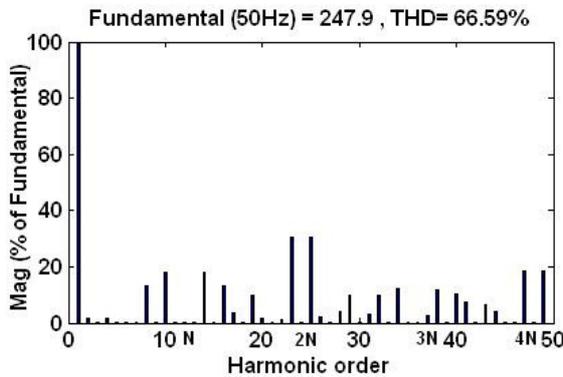


Figure 7 Harmonics spectrum of 7-segment SVM with $N=12$

5. Experiment results

When SVM control technique is used in the power electronic system, it mostly operates in the linearity region. So the experiment was conducted with $m=1$ and $V_d=310V$ in the linearity region to test the DC bus voltage utilization. Figure 8 and Figure 9 show the test results. The output line voltage magnitude of the proposed SVM and 7-segment SVM all can reach the maximum value V_d . The proposed SVM can increase the utilization of DC bus voltage, which agrees with the simulation results.

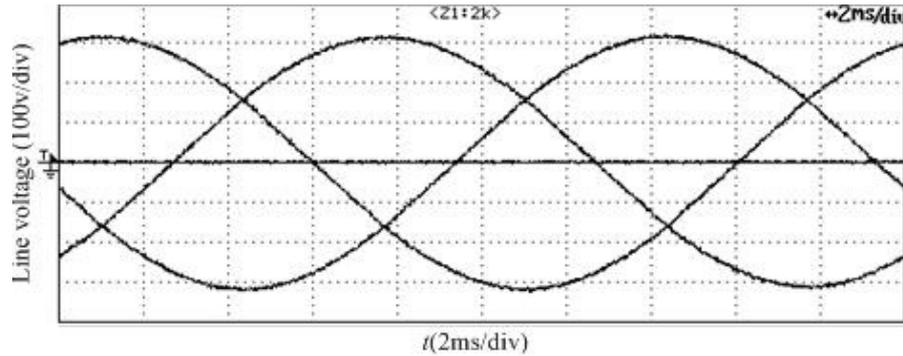


Figure 8 Proposed SVM test waveforms of line voltage with $m=1$

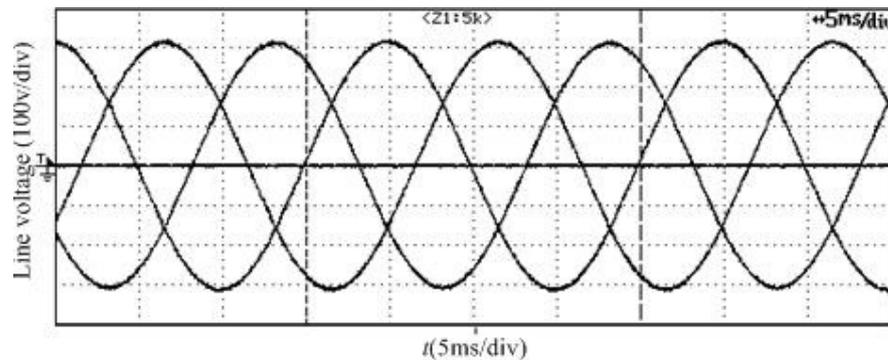
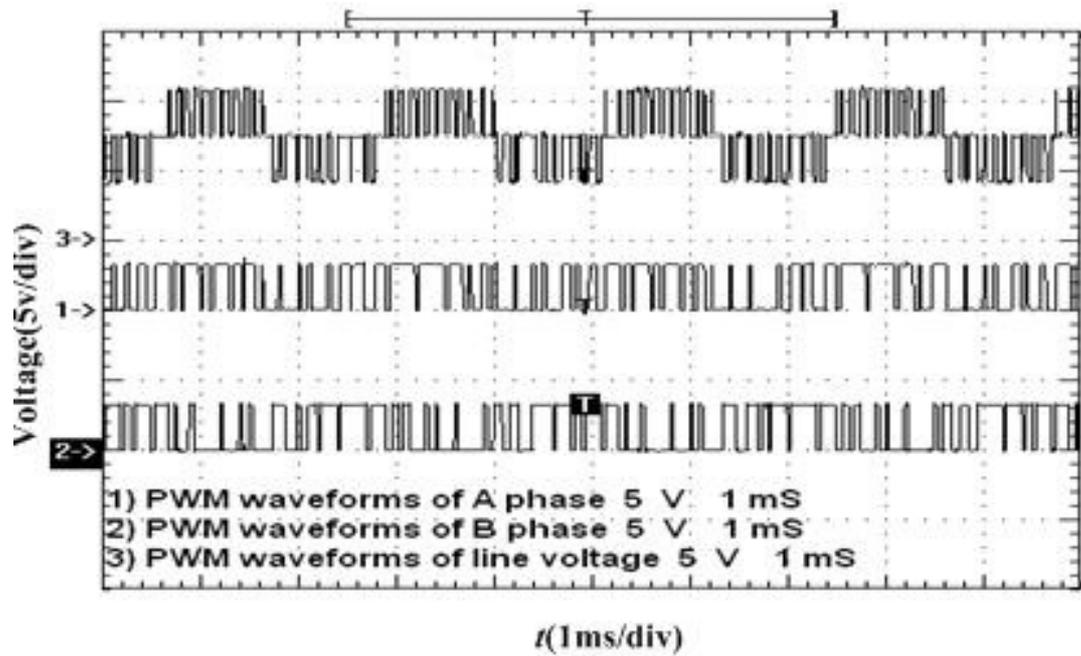


Figure 9 7-segment SVM test waveforms of line voltage with $m=1$

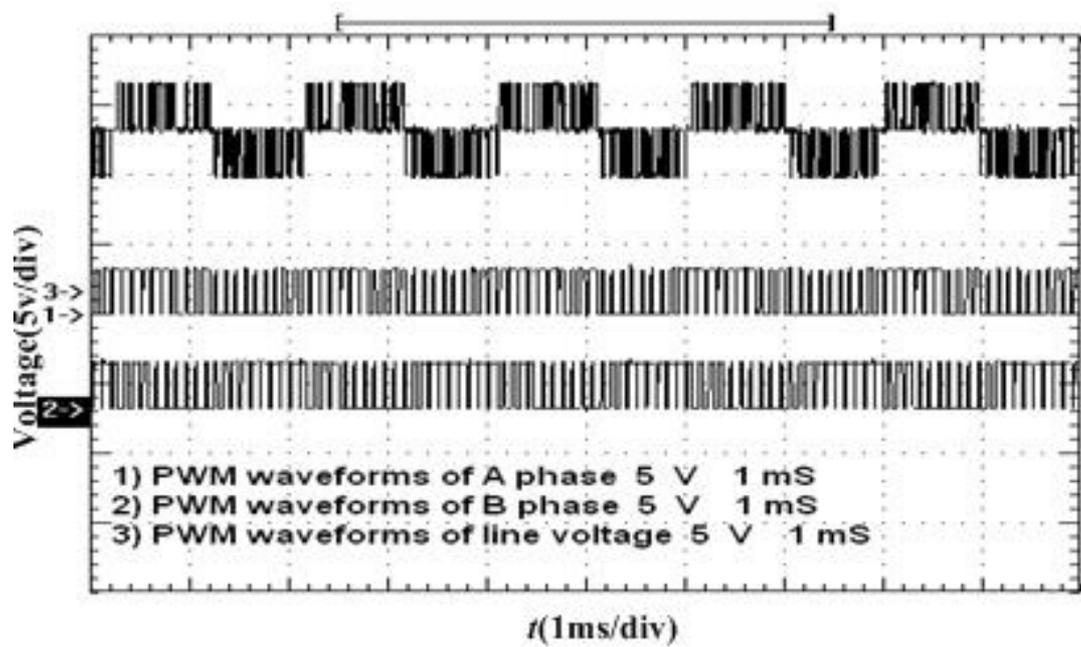
Further experiments had been carried out to prove the validity of optimal switching sequence by using TMS320F2812 DSP. Parameters are given as follows: $m=0.7$, $T_s=10\mu s$, $T=1.8ms$ (T_s : sample time, T : output voltage periods).

Both 7-segment SVM and the proposed SVM experimental results were shown in Figure 10. The waveforms of 1 and 2 channel in the figure were the PWM driving waveforms of A and B phase. It is clear that the switching times of the proposed SVM are less than the 7-segment SVM under the same sample time. As a result, the switching losses of proposed SVM will reduce obviously.

The experiments also show that the proposed SVM can use smaller filter than the conventional 7-segment SVM to control harmonics of the output line voltage. This means that THD of the proposed SVM is less than that of 7-segment SVM with the same switching frequency.



(a) Proposed SVM



(b) 7-segment SVM

Figure 10 PWM waveforms

6. Conclusion

SVM is a popular choice in the inverter or rectifier controls. A novel SVM was presented. It can obtain the same output voltage in linearity modulation or overmodulation region compared to 7-segment SVM. Moreover, it can make doubled calculation at specified switching frequency, i.e. it reduces the switching losses under the same sampling time, compared to the conventional SVM scheme. And it performs better in terms of THD of the output line voltage under the same switching frequency. The simulation and experimental results demonstrate the validity and efficiency of the proposed control scheme.

Acknowledgments

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